

NCP1501

Dual Mode PWM/Linear Buck Converter

The NCP1501 is a dual mode regulator that operates either as a PWM Buck Converter or as a Low Drop Out Linear Regulator. If a synchronization signal is present, the NCP1501 operates as a current mode PWM converter with synchronous rectification. The synchronization signal allows the user to control the location of the spurious frequency noise generated by a PWM converter. Linear mode is active when a synchronization signal is not present. The NCP1501 configuration allows an efficient high power operation and low noise during system sleep modes.

Features

- Synchronous Rectification for Higher Efficiency in PWM Mode
- Linear Mode Operation for Low Noise Output at Low Loads
- Integrated MOSFETs and Feedback Circuits
- Cycle-by-Cycle Peak Current Limit of 800 mA (typ)
- Automatic Switching Between PWM and Linear Mode
- Operating Frequency Range of 500 to 1000 kHz
- Optimized for Ceramic Capacitors and Low Profile Inductors
- Thermal Limit Protection
- Built-in Slope Compensation for Current Mode PWM Converter
- Fixed Output Voltages of 1.05 V, 1.35 V, 1.57 V, 1.8 V
- Shutdown Current Consumption of 0.2 μ A
- Internal Soft Start
- Transistor Count: 3500
- Pb-Free Package is Available

Typical Applications

- Cellular Phones
- PDAs
- Pagers
- Supplies for DSP Cores
- Portable Applications

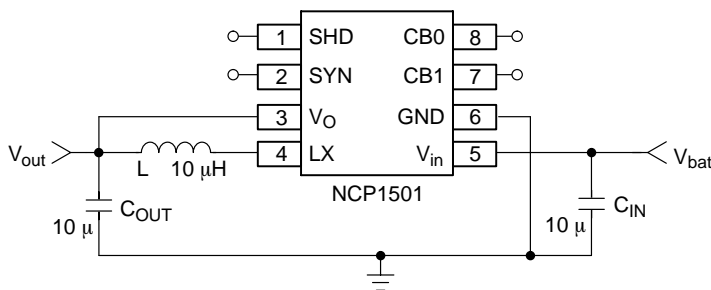


Figure 1. Typical Applications Circuit



ON Semiconductor®

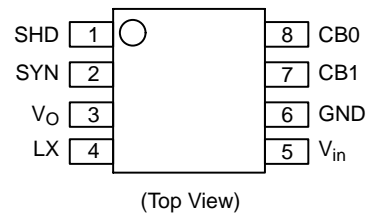
<http://onsemi.com>

MARKING DIAGRAM



1501 = Device Code
 A = Assembly Location
 Y = Year
 W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1501DMR2	Micro8	4000/Tape & Reel
NCP1501DMR2G	Micro8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP1501

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	SHD	Enable Pin for the NCP1501. This pin is active high. Internal pull down resistor forces the part off if the pin is not connected on the board.
2	SYN	External Synchronization Signal Pin. The device will operate in PWM mode if a clock signal is present. The pin must be pulled low to enter LDO mode. Internal pull down resistor on pin.
3	V _O	Feedback for the NCP1501. An internal MOSFET is connected across V _O and LX for LDO mode.
4	LX	Connection for the pass devices to the inductor.
5	V _{in}	Input voltage to the NCP1501.
6	GND	Ground Connection for the device.
7	CB1	Voltage Selection Bit. Internal pull up resistor on pin.
8	CB0	Voltage Selection Bit. Internal pull down resistor on pin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Maximum Voltage All Pins	V _{max}	5.5	V
Maximum operating Voltage All Pins	V _{max}	5.2	V
Thermal Resistance, Junction-to-Air	R _{θJA}	240	°C/W
Operating Ambient Temperature Range	T _A	-30 to +85	°C
ESD Withstand Voltage	V _{ESD}	> 2500 > 100	V
		Human Body Model (Note 1) Machine Model (Note 2)	
Moisture Sensitivity	MSL	Level 1	
Storage Temperature Range	T _{stg}	-55 to +150	°C
Junction Operating Temperature Range	T _J	-30 to +125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A

ELECTRICAL CHARACTERISTICS (V_{in} = 3.6 V, V_O = 1.57 V, T_A = 25°C, F_{syn} = 600 kHz 50% Duty Cycle square wave for PWM mode; T_A = -30 to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

V_{CC} Pin

Quiescent Current of Switching Mode, I _{out} = 0 mA	I _q PWM	-	124	500	μA
Quiescent Current of LDO Mode, I _{out} = 0 mA	I _q LDO	-	32	65	μA
Quiescent Current, SHD Low	I _q Off	-	0.2	1.0	μA
Input Voltage Range	V _{in}	2.7	-	5.2	V

Sync Pin

Input Voltage	V _{sync}	-0.3	-	V _{CC} +0.3	V
Frequency Operational Range	F _{sync}	500	-	1000	kHz
Minimum Synchronization Pulse Width	DC _{sync(min)}	-	30	-	%
Maximum Synchronization Pulse Width	DC _{sync(max)}	-	70	-	%
SYNC "H" Voltage Threshold	V _{sync(H)}	-	920	1200	mV
SYNC "L" Voltage Threshold	V _{sync(L)}	400	830	-	mV
SYNC "H" Input Current, V _{sync} = 3.6 V	I _{sync(H)}	-	1.8	-	μA
SYNC "L" Input Current, V _{sync} = 0 V	I _{sync(L)}	-0.5	0.005	-	μA

NCP1501

ELECTRICAL CHARACTERISTICS (continued) ($V_{in} = 3.6\text{ V}$, $V_O = 1.57\text{ V}$, $T_A = 25^\circ\text{C}$, $F_{syn} = 600\text{ kHz}$ 50% Duty Cycle square wave for PWM mode; $T_A = -30$ to 85°C for Min/Max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Output Level Selection Pins

Input Voltage	V_{CB}	-0.3	-	$V_{CC}+0.3$	V
CB0,1 "H" Voltage Threshold	$V_{CB(H)}$	-	910	1200	mV
CB0,1 "L" Voltage Threshold	$V_{CB(L)}$	400	850	-	mV
CB0,1 "H" Input Current, $CBx = 3.6\text{ V}$	$I_{CB(H)}$	-	1.8	-	μA
CB0,1 "L" Input Current, $CBx = 0\text{ V}$	$I_{CB(L)}$	-0.5	0	-	μA

Shutdown Pin

Input Voltage	V_{SHD}	-0.3	-	$V_{CC}+0.3$	V
SHD "H" Voltage Threshold	$V_{SHD(H)}$	-	920	1200	mV
SHD "L" Voltage Threshold	$V_{SHD(L)}$	400	850	-	mV
SHD "H" Input Current, $SHD = 3.6\text{ V}$	$I_{SHD(H)}$	-	1.8	-	μA
SHD "L" Input Current, $SHD = 0\text{ V}$	$I_{SHD(L)}$	-0.5	0	-	μA

Feedback Pin

Input Voltage	V_{fb}	-0.3	-	$V_{CC}+0.3$	V
Input Current, $V_{fb} = 1.8\text{ V}$	I_{fb}	-	8.5	-	μA

PWM Mode Characteristics

Switching P-FET Current Limit	I_{lim}	-	800	-	mA
Duty Cycle	DC	-	-	100	%
Minimum On Time	$T_{on(min)}$	-	100	-	nsec
$R_{DS(on)}$ Switching N-FET P-FET	$R_{DS(on)}$	-	0.7 0.6	-	Ohms
Switching P-FET and N-FET Leakage Current	I_{leak}	-	0.01	10	μA
Output Over Voltage Threshold	V_O	-	3.0	-	%
Output Voltage Accuracy, $V_{out(set)} = 1.05\text{ V}$ $CB0 = L$, $CB1 = L$ $V_{out(set)} = 1.35\text{ V}$ $CB0 = L$, $CB1 = H$ $V_{out(set)} = 1.57\text{ V}$ $CB0 = H$, $CB1 = H$ $V_{out(set)} = 1.80\text{ V}$ $CB0 = H$ $CB1 = L$	V_{out}	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V
Load Transient Response, 10 to 100 mA Load Step	V_{out}	-	40	-	mV
Line Transient Response, $I_{out} = 100\text{ mA}$, 3.0 to 3.6 V_{in} Line Step	V_{out}	-	± 5	-	mV _{pp}

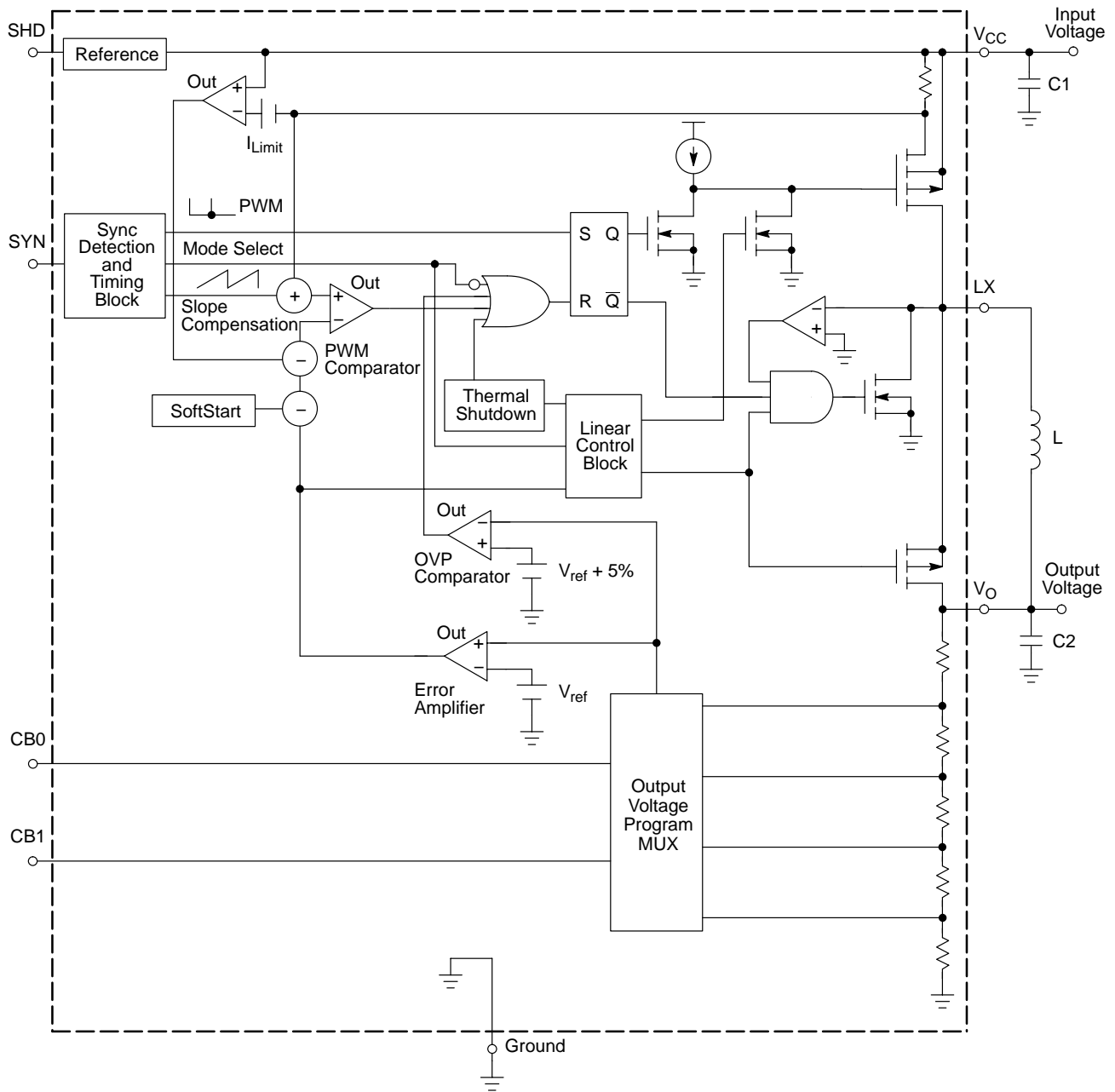
LDO Mode Characteristics

$R_{DS(on)}$ LDO FET (Inductor Switch), LX to V_{out}	$R_{DS(on)}$	-	7.0	-	Ohms
Dropout Voltage (Limited by $V_{in(min)} = 2.5\text{ V}$ and $V_{out(max)} = 1.8\text{ V}$)	$V_{in} - V_{out}$	-	0.7	-	V
Output Voltage Accuracy, $V_{out(set)} = 1.05\text{ V}$ $CB0 = L$, $CB1 = L$ $V_{out(set)} = 1.35\text{ V}$ $CB0 = L$, $CB1 = H$ $V_{out(set)} = 1.57\text{ V}$ $CB0 = H$, $CB1 = H$ $V_{out(set)} = 1.80\text{ V}$ $CB0 = H$ $CB1 = L$	V_{out}	1.018 1.309 1.523 1.740	1.050 1.350 1.570 1.800	1.082 1.391 1.617 1.860	V

Thermal Shutdown

Thermal Shutdown	TSD	-	160	-	$^\circ\text{C}$
Hysteresis	TSD _{hys}	-	25	-	$^\circ\text{C}$

NCP1501



Component	Value	Manufacturer
C1, C2	10 μ F, 6.3 V	TDK, C2012X5R0J106M (0805 size)
L	10 μ H	TDK, LLF4017-100 ($I_{out} = 300$ mA) Coilcraft, LPO4812-103MX ($I_{out} = 300$ mA) Coilcraft, 0805PS-103M ($I_{out} = 150$ mA) TDK, NLC252018T-100 ($I_{out} = 100$ mA)

Figure 2. Typical Circuit with the Internal Schematic

NCP1501

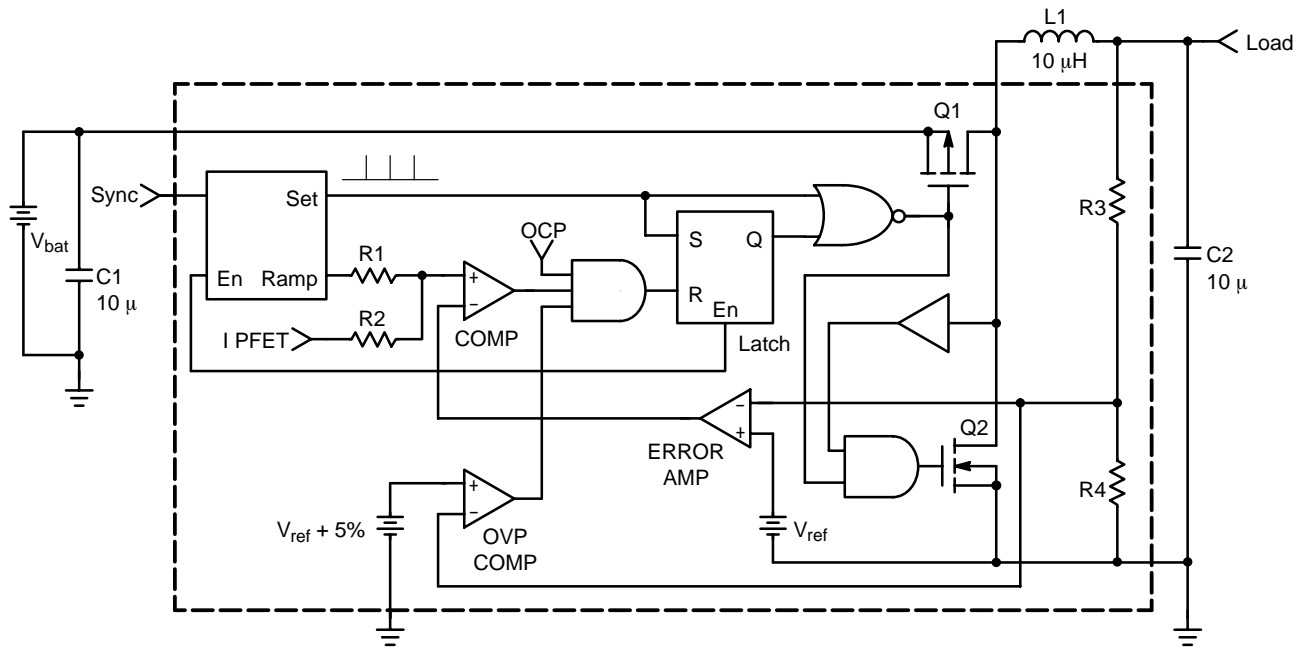


Figure 4. PWM Circuit Schematic

LDO Mode

When the synchronization pulse is not present, the NCP1501 operates as an LDO. The DC/DC Control Circuitry will relinquish control of Q1 and turn off Q2. The

LDO Control Circuitry will turn on Q3 as a bypass circuit to the inductor. Q1 is the controlling pass device of the LDO that regulates the input to output voltage dropout. The LDO can source an output current in excess of 50 mA.

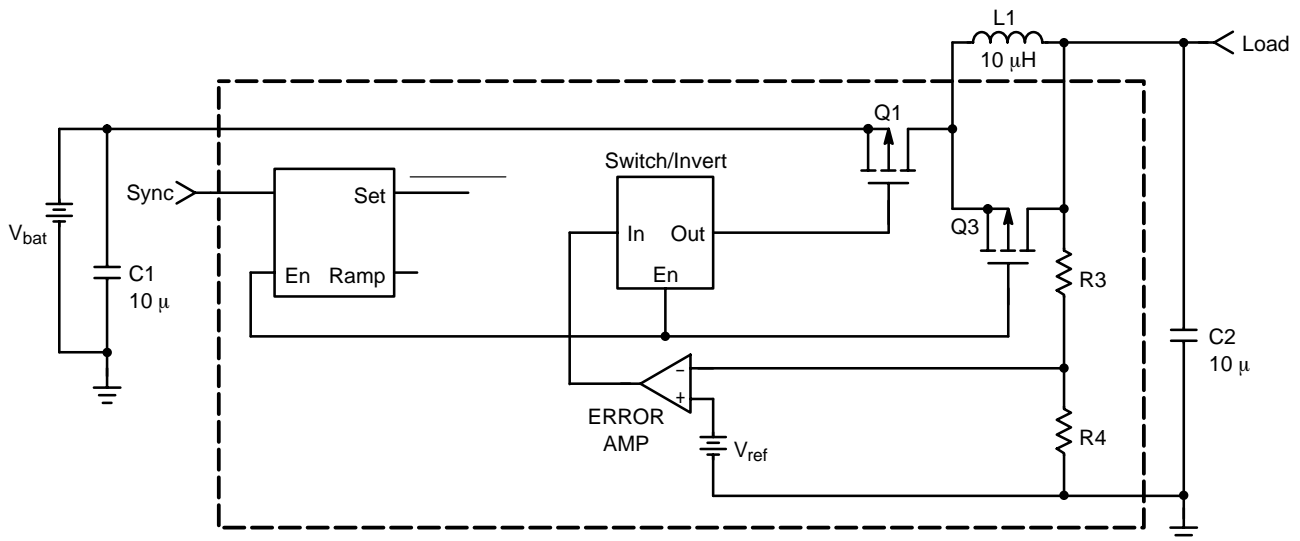


Figure 5. LDO Circuit Schematic

NCP1501

Voltage Output Selection

The output voltage selection is accomplished via two external pins: CB0 and CB1. If CB0 and CB1 pins are left floating by the external circuit, the output voltage will default to 1.35 V. The corresponding voltages are as follows.

		NCP1501	
CB0	CB1	V _{out} (V)	
0	0	1.05	
0	1	1.35	
1	1	1.57	
1	0	1.80	

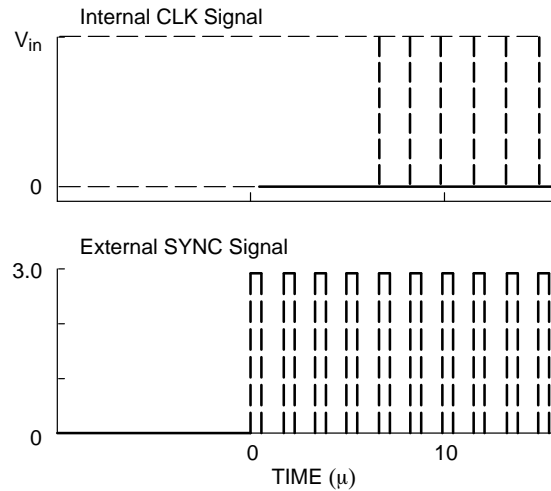


Figure 6. Transition Waveforms from LDO to PWM Mode

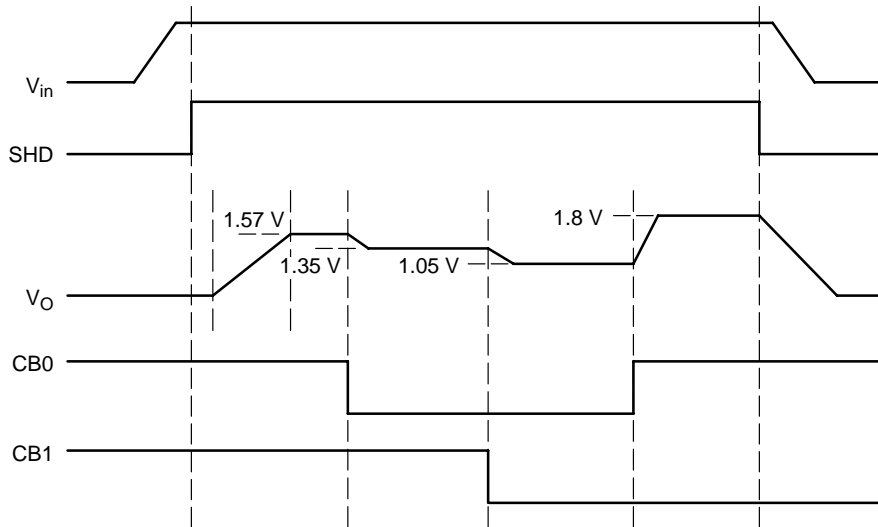


Figure 7. Power Up and Power Down Sequence

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM latch is reset and the linear regulator control circuitry is disabled. The thermal shutdown circuit is designed with 25°C of hysteresis. This means that the

PWM latch and the regulator control circuitry cannot be re-enabled until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended as a substitute for proper heatsinking. The NCP1501 is contained in the Micro-8 package.

NCP1501

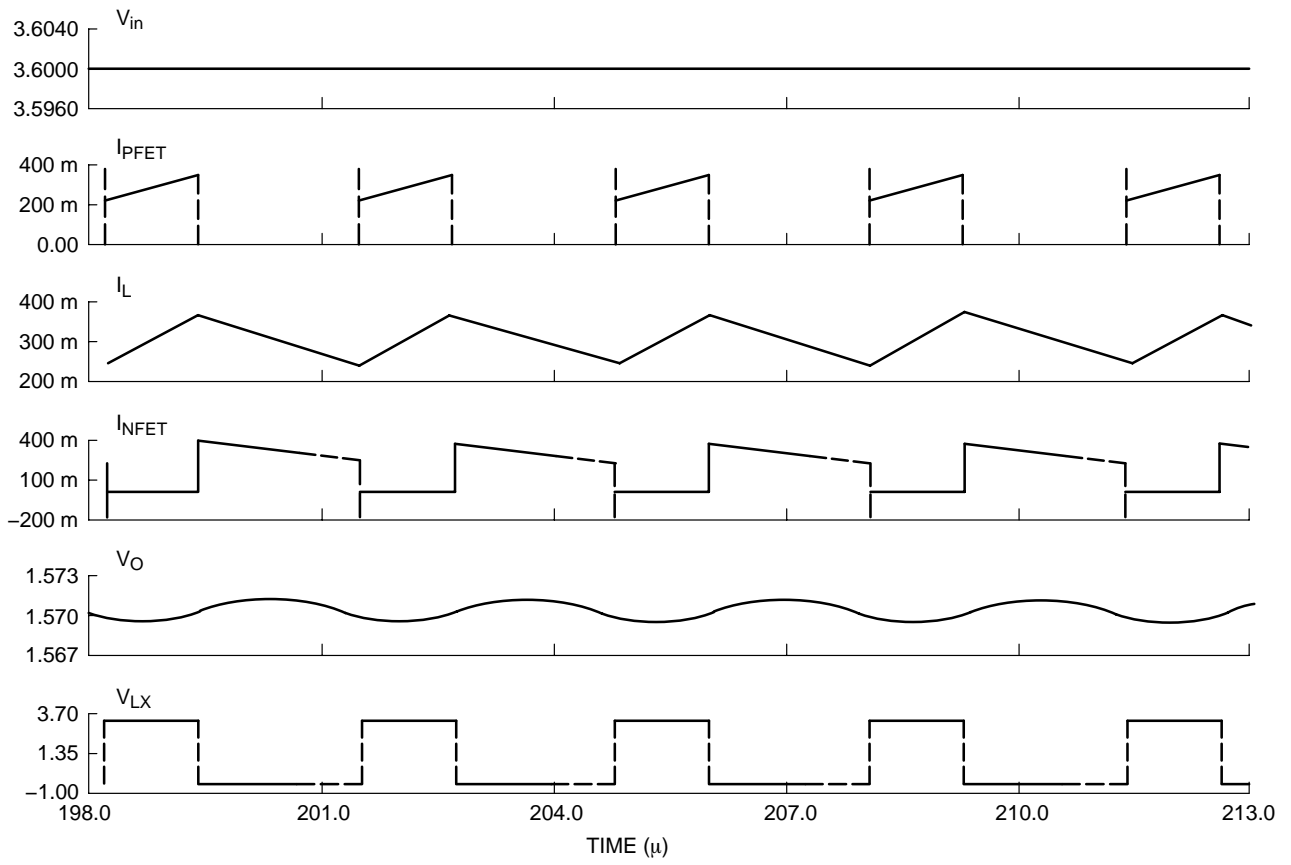


Figure 8. Waveforms During Normal Operation

NCP1501

APPLICATIONS INFORMATION

NCP1501 is a dual mode PWM or LDO step down converter. This dual mode takes advantage of the best of each mode. There are three required external components: an input and output capacitor and an inductor.

The PWM mode allows high efficiency for larger loads. A typical efficiency for an input of 3.6 V and an output of 1.8 V and 100 mA is over 90%. Low $R_{DS(on)}$ and synchronous rectification contained within the device contributes to the very high efficiency. As with other synchronous rectification devices, the NCP1501 does not require an external diode to supplement the NFET during switching on or off. A synchronization pin allows the user to define the frequency noise spikes of the PWM. The duty cycle of the synchronization signal must be within the range

of 30% to 70%. The rising edge of the signal from the synchronization pin acts as the oscillator signal to set the latch and reset the ramp compensation signal. An Over Voltage Protection circuit ensures the output will respond properly to fast transients from large to small loads. The NCP1501 allows the PWM mode to enter a 100% duty cycle for fast load transient conditions and low input to output voltage differentials.

The LDO mode is effective during low load conditions by lowering the quiescent current and reducing the output ripple voltage associated with PWM converters entering PFM mode. NCP1501 enters the LDO mode when a synchronization signal is not present. It is recommended to pull the synchronization signal low for LDO mode.

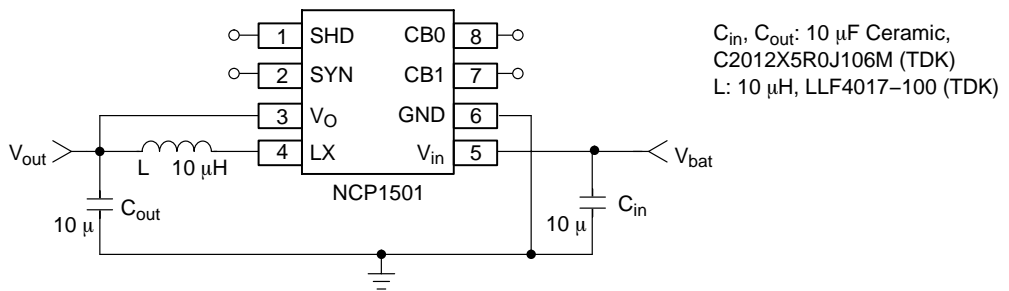


Figure 9. Typical Operating Schematic

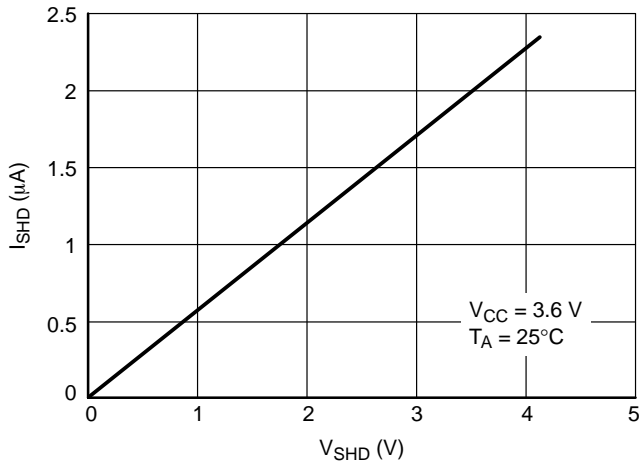


Figure 10. Input Current versus Voltage for the Shutdown Pin

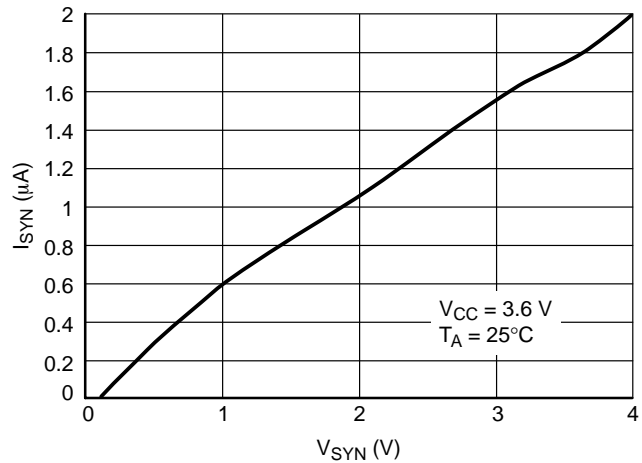


Figure 11. Input Current versus Voltage for the Synchronization Pin

NCP1501

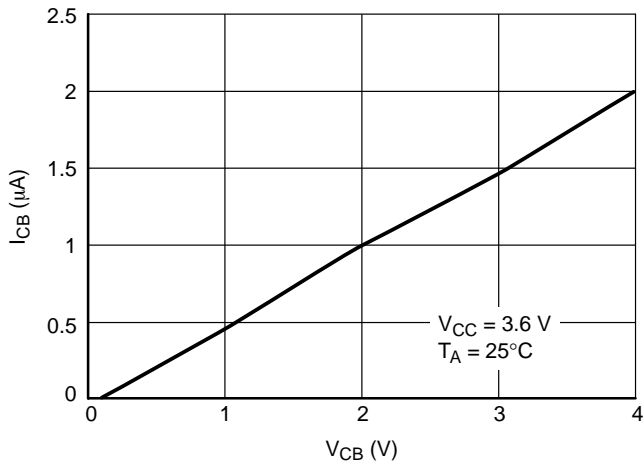


Figure 12. Input Current versus Voltage for the CB Pins

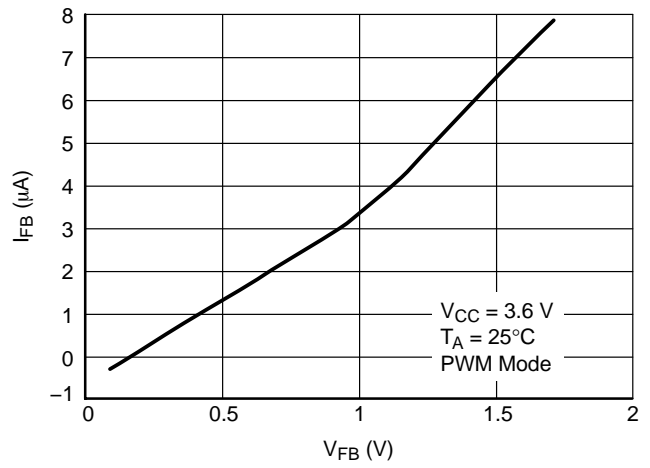


Figure 13. Input Current versus Voltage for the Feedback Pin

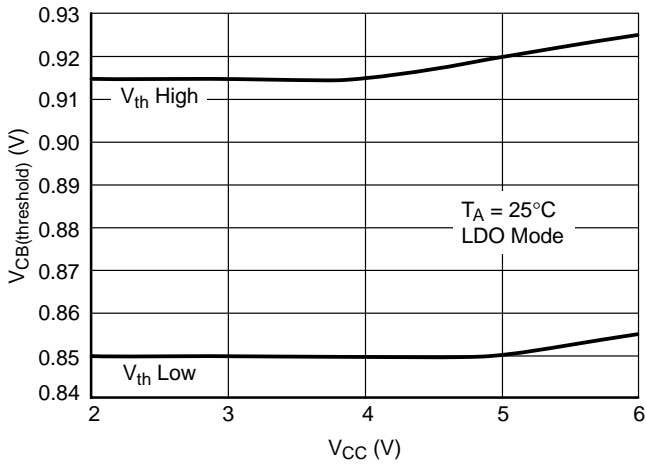


Figure 14. V_{CC} Input Voltage versus CB Threshold

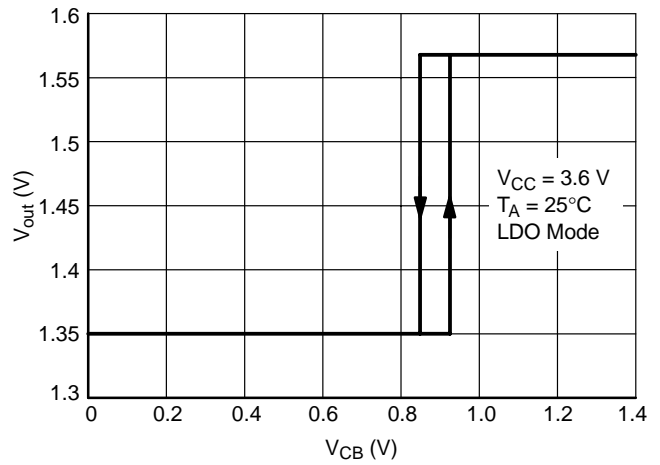


Figure 15. Transition Level of CB Pins

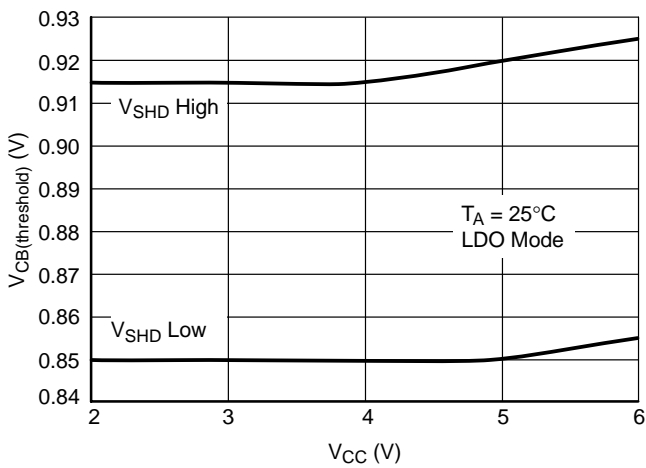


Figure 16. Input Voltage versus Shutdown Voltage

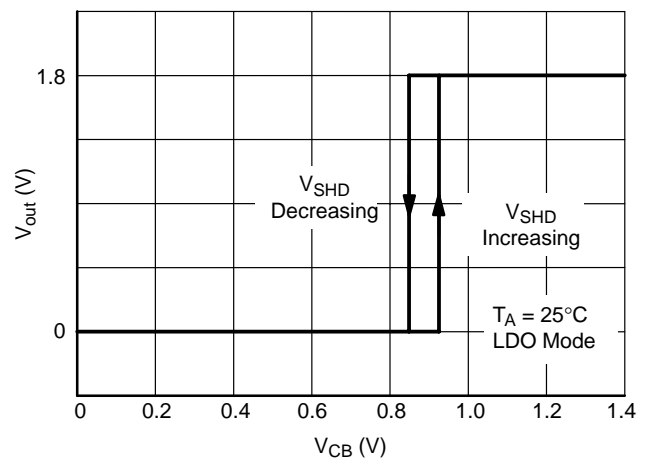


Figure 17. Output Voltage versus Shutdown Pin Voltage

NCP1501

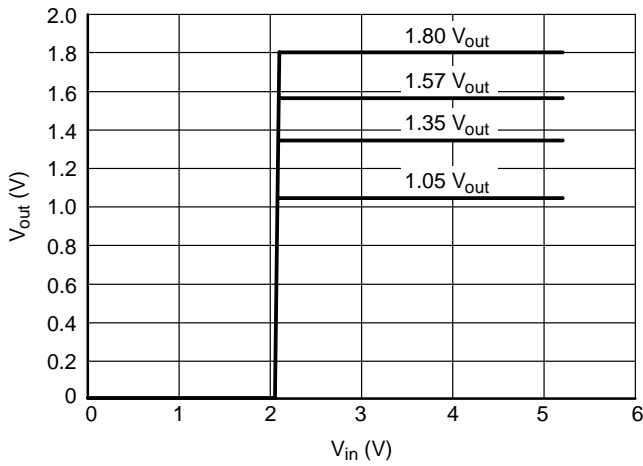


Figure 18. Output Voltage versus PWM Input Voltage

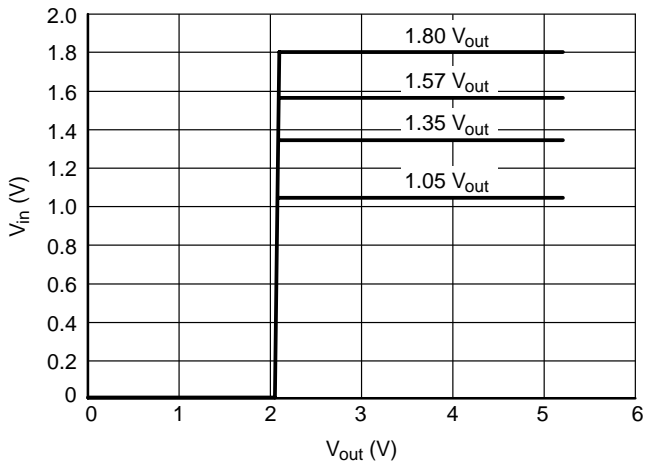


Figure 19. Input Voltage versus Output Voltage

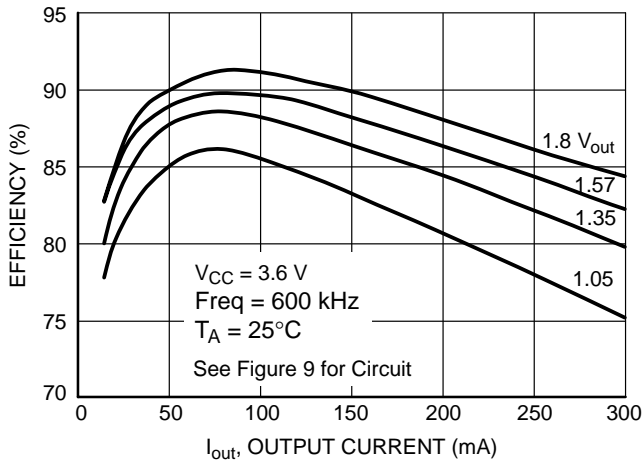


Figure 20. Efficiency versus Output Current

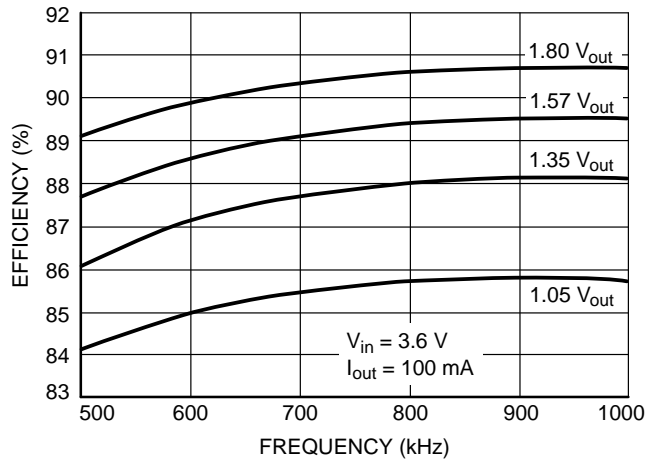


Figure 21. Efficiency versus Frequency

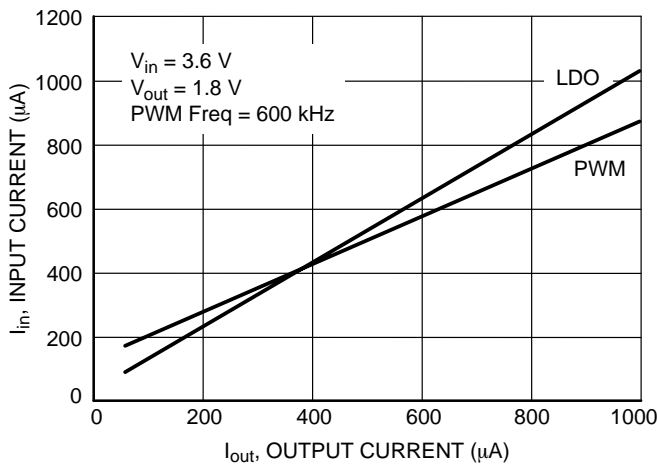


Figure 22. Input Current versus Output Current Comparison for PWM and LDO Mode

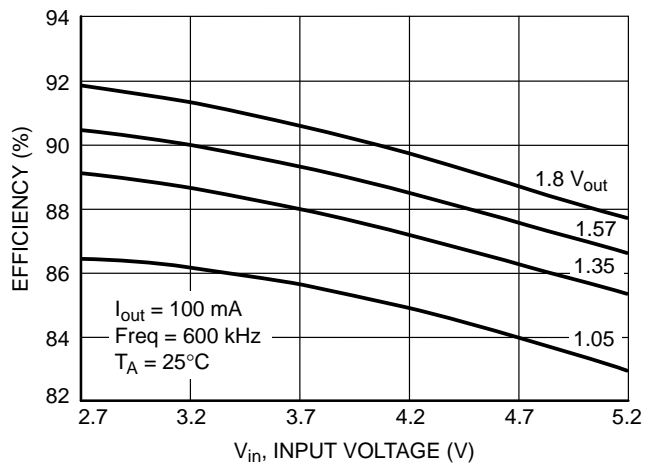


Figure 23. Efficiency versus Input Voltage

NCP1501

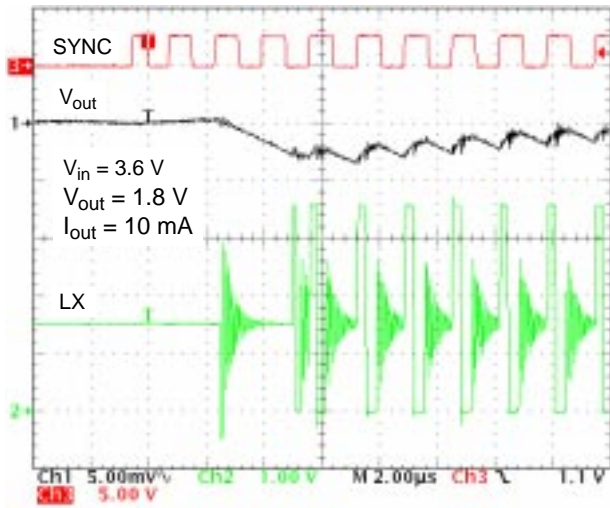


Figure 24. Transition from LDO to PWM Mode

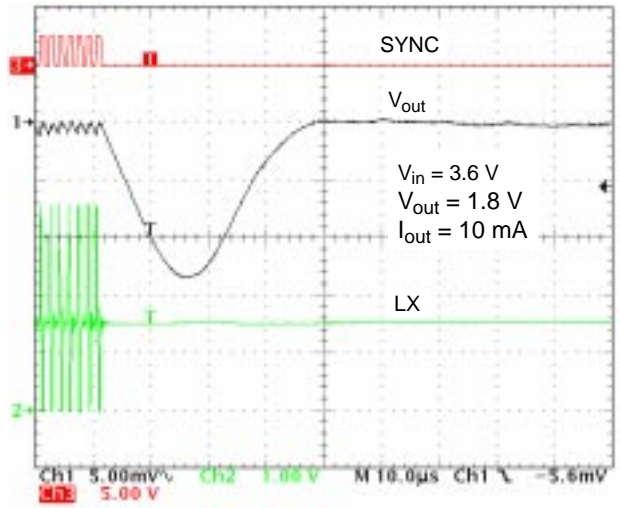


Figure 25. Transition from PWM to LDO Mode

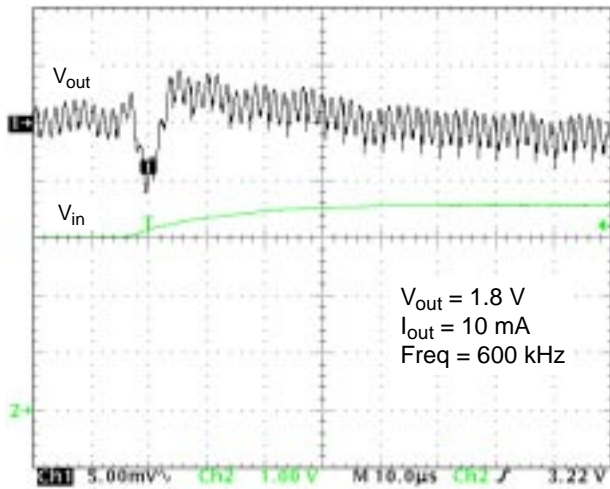


Figure 26. Line Transient from 3.0 to 3.6 V

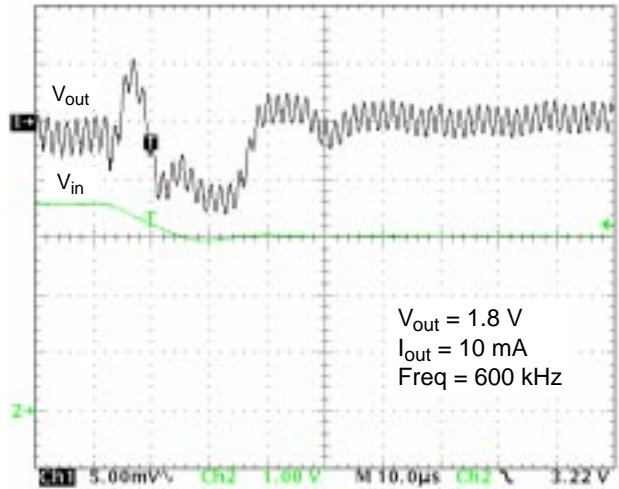


Figure 27. Line Transient from 3.6 to 3.0 V

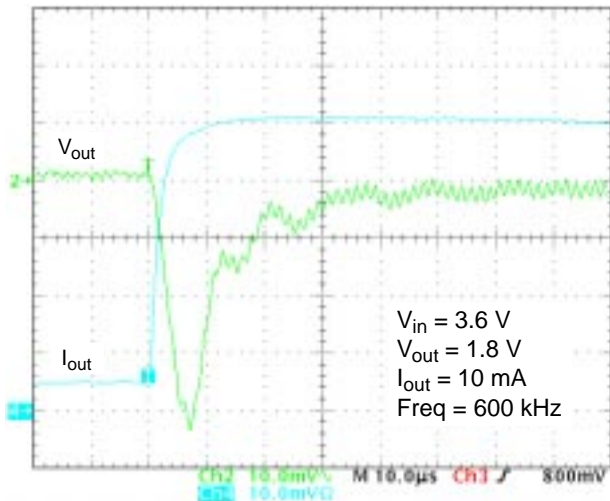


Figure 28. Load Transient from 10 to 100 mA

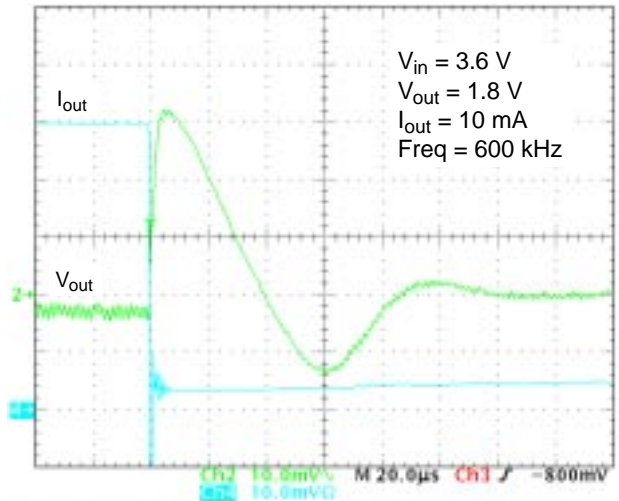


Figure 29. Load Transient from 100 to 10 mA

NCP1501

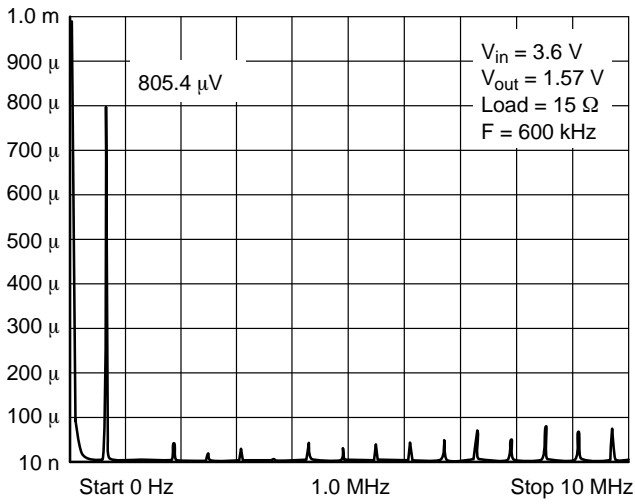


Figure 30. V_{rms} versus Frequency

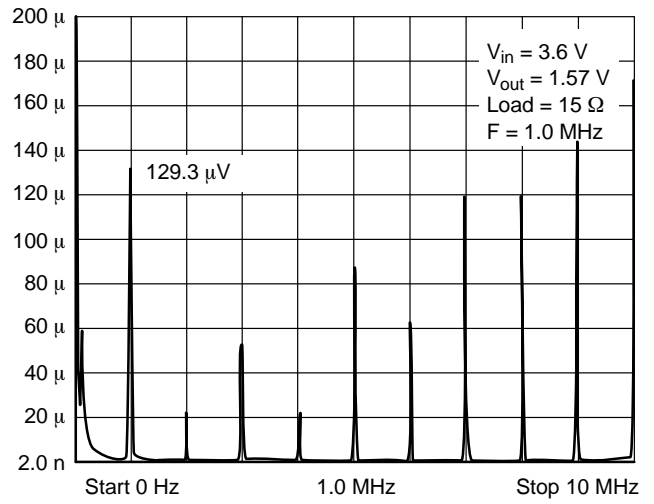


Figure 31. V_{rms} versus Frequency

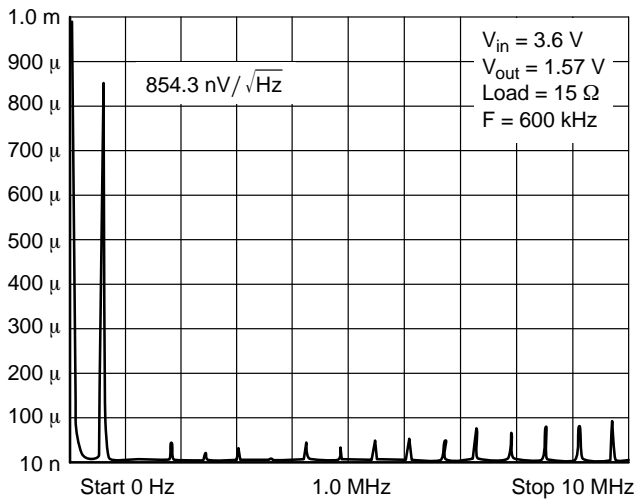


Figure 32. Noise versus Frequency

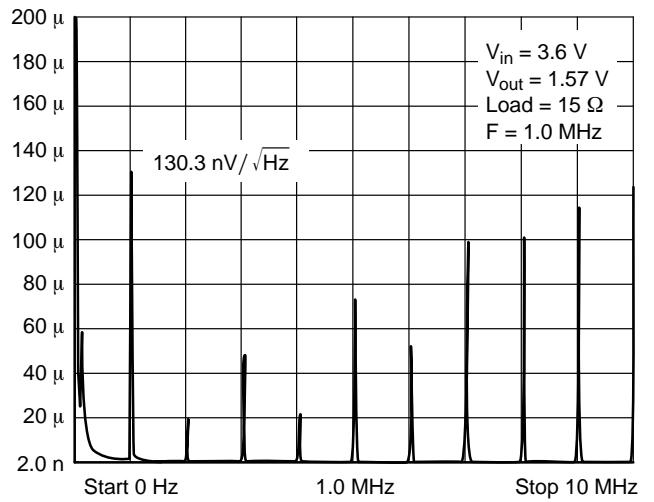
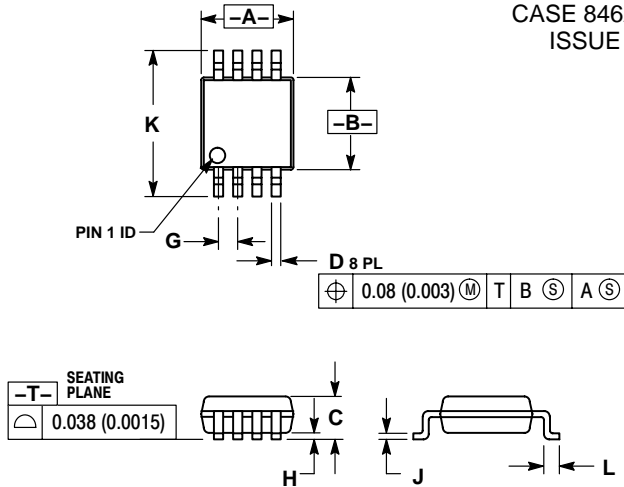


Figure 33. V_{RMS} versus Frequency

NCP1501

PACKAGE DIMENSIONS

**Micro8
(MSOP-8)
DM SUFFIX
CASE 846A-02
ISSUE F**

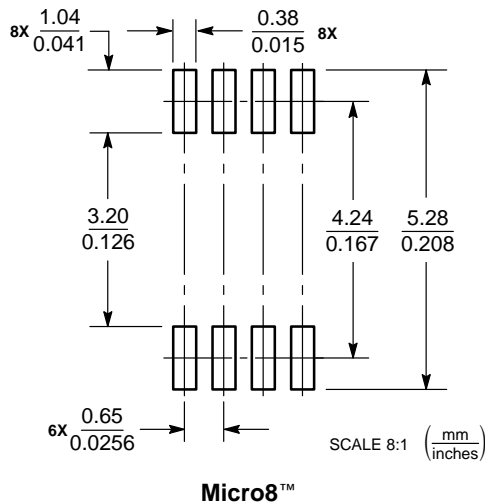


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Micro8 is a trademark of International Rectifier.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>
Order Literature: <http://www.onsemi.com/litorder>
For additional information, please contact your local Sales Representative.